

SiGe/Si Solid State Power Amplifiers

P. Bhattacharya and L. P. B. Katehi

Department of Electrical Engineering and Computer Science
University of Michigan, Ann Arbor, MI 48109-2122

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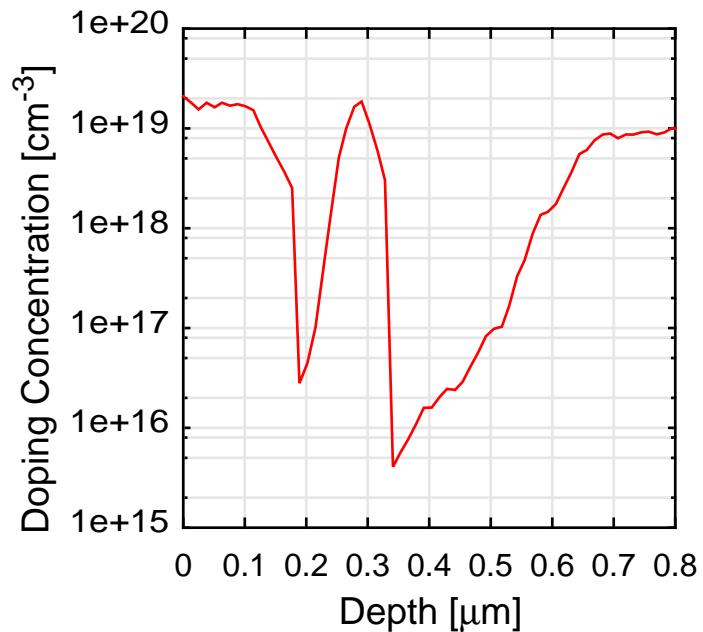
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SiGe/Si HBT Epitaxial Structure

- Structure

Emitter Contact	Si	n+	1e19	2000 Å
Emitter	Si	n	2e18	1000 Å
Spacer	SiGe	i		50 Å
Base	Si _{1-x} Ge _x	p+	1e20	200 Å
Spacer	SiGe	i		50 Å
Collector	Si	n-	5e15	3000 Å
Subcollector	Si	n+	1e19	1.5 μm
Substrate	Si	p-	2e12	540 μm

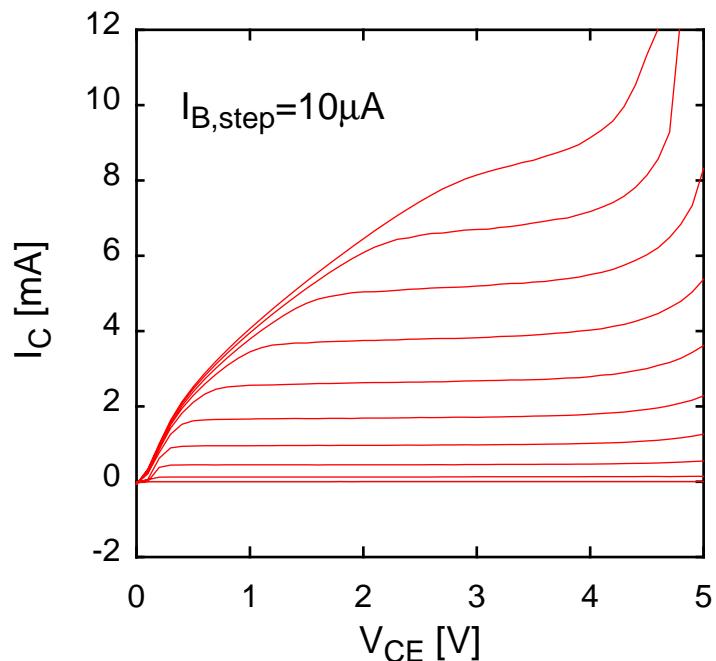
- SRA measurement



- All layers grown by MBE except for subcollector layer(CVD)
- $r_{growth} = 2\text{ Å/sec}$ for emitter and collector, 0.8 Å/sec for base
- $T_{growth} = 415^\circ\text{C}$ for emitter and collector, 550°C for base
- $P_{background} = 6 \times 10^{-9}$ torr

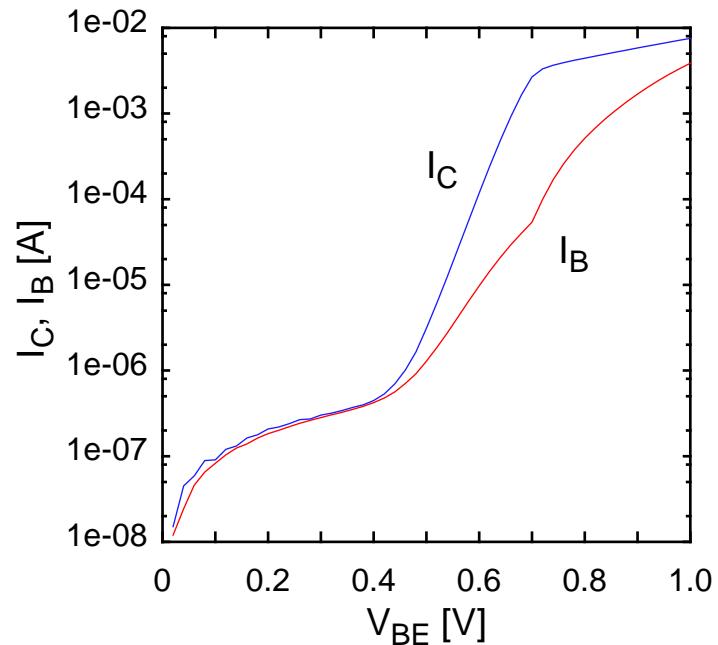
Characteristics of Fabricated SiGe/Si HBT

- I-V Characteristics



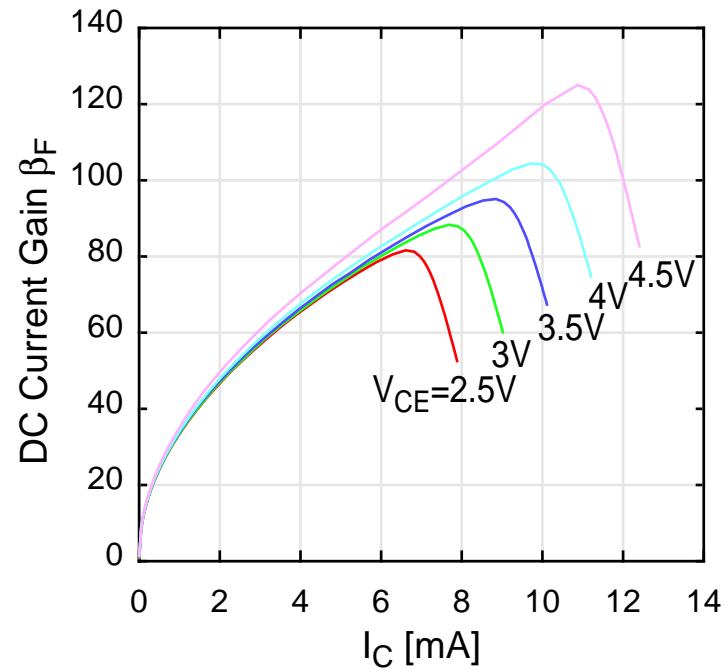
- $A_E = 5 \times 5 \mu\text{m}^2$, $A_{BC} = 12 \times 13 \mu\text{m}^2$
- $BV_{CEO} \sim 5 \text{ V}$
- Kirk effect at low V_{CE}

- Gummel Plot



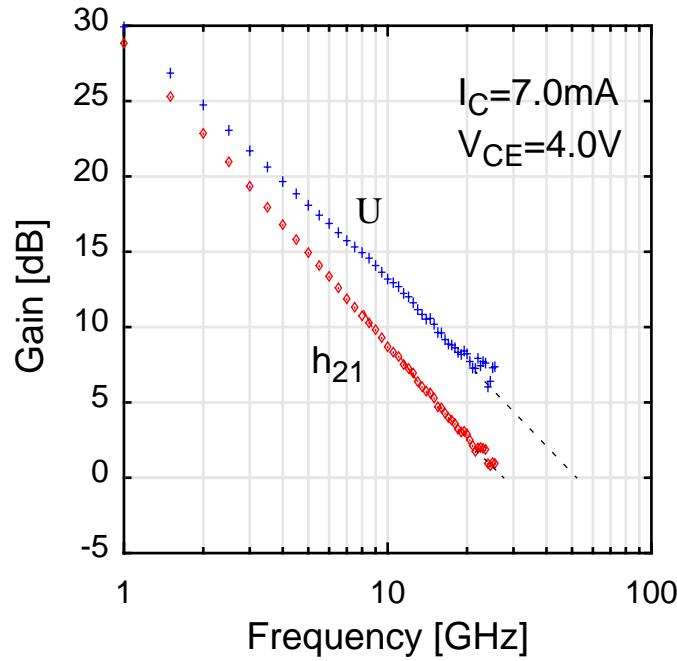
- $n_C = 1.04$, $n_B = 1.79$

• Current Gain



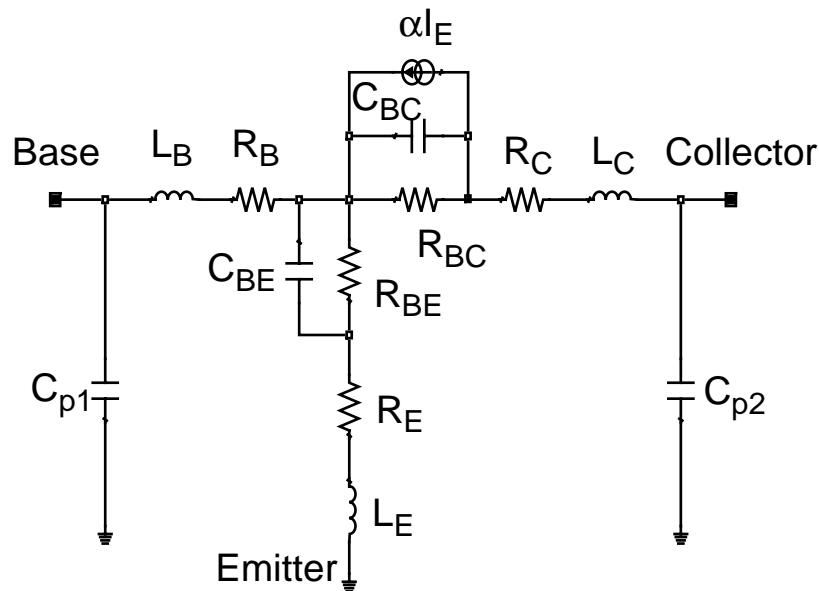
- β_F (DC gain) ~100
- β_0 (Differential gain) ~200

• Frequency Response



- $f_T = 28.0 \text{ GHz}$
- $f_{max} = 51.8 \text{ GHz}$

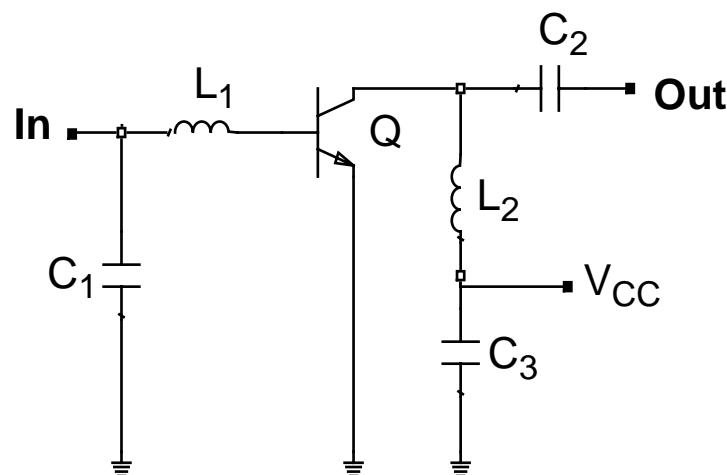
Small Signal Model of SiGe/Si HBT



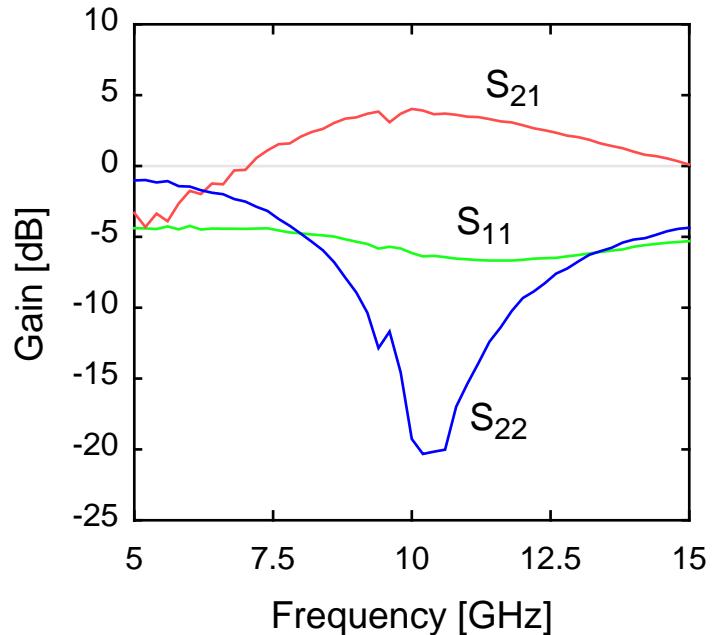
V_{CE}	4 V
I_C	7.4 mA
I_B	80 μ A
R_B	13.1 Ω
L_B	62.6 pH
R_{BE}	1.0 Ω
C_{BE}	106.8 fF
R_E	15.8 Ω
L_E	141.7 pH
R_{BC}	127.0 k Ω
C_{BC}	28.9 fF
R_C	24.8 Ω
L_C	66.1 pH
$C_{p1,2}$	4.0 fF
α_o	0.995

Single-stage X-band SiGe/Si Monolithic Amplifier

- Circuit Schematic



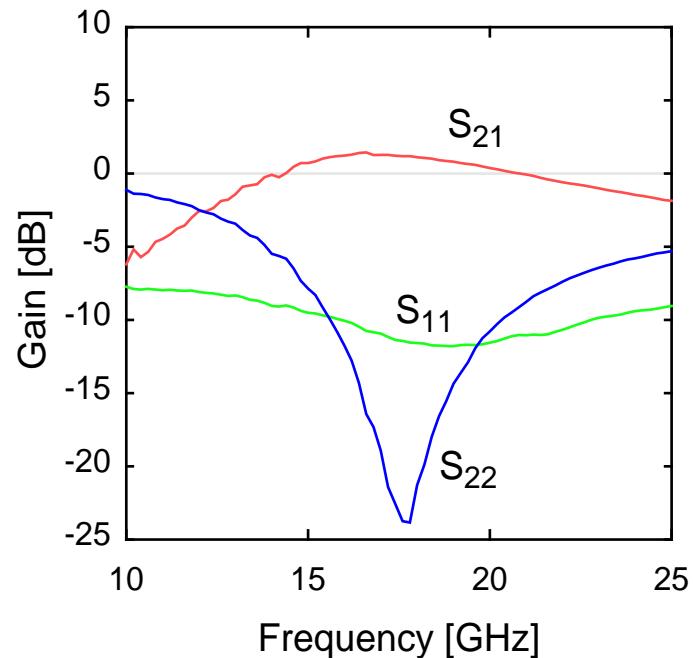
- Gain and Return Losses



- $S_{21}=4.03 \text{ dB} @ 10.0 \text{ GHz}$
- $\text{VSWR}_{\text{in}}=2.73$
- $\text{VSWR}_{\text{out}}=1.21$

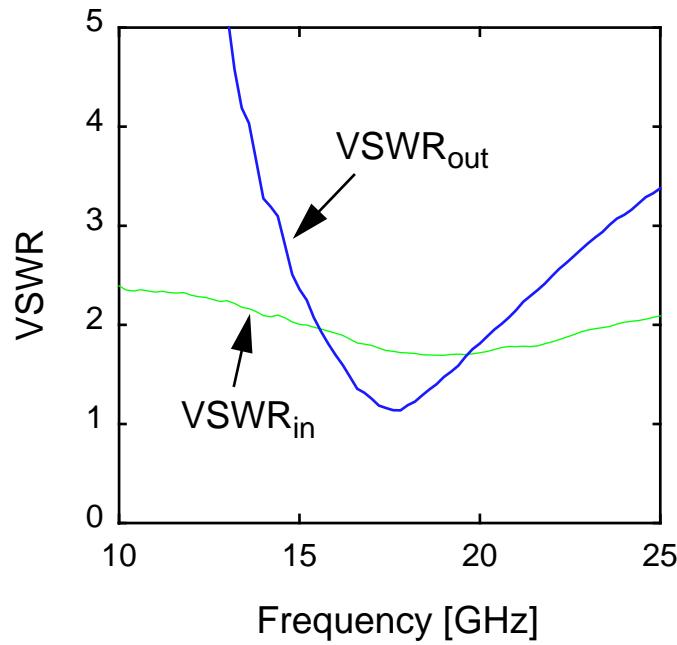
Single-stage Ku-band SiGe/Si Monolithic Amplifier

- Gain and Return Losses



► $S_{21}=1.44 \text{ dB @ } 16.6 \text{ GHz}$

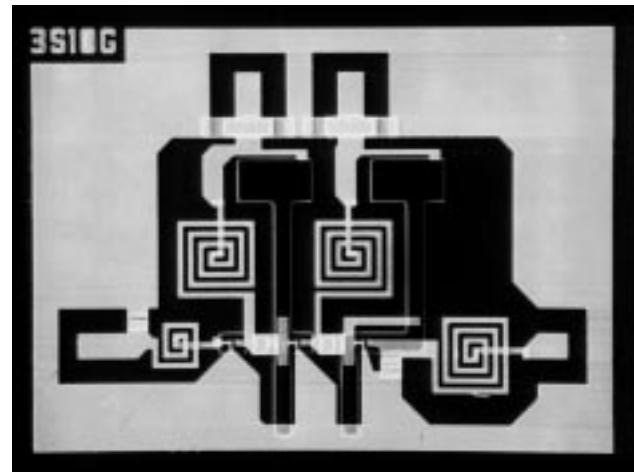
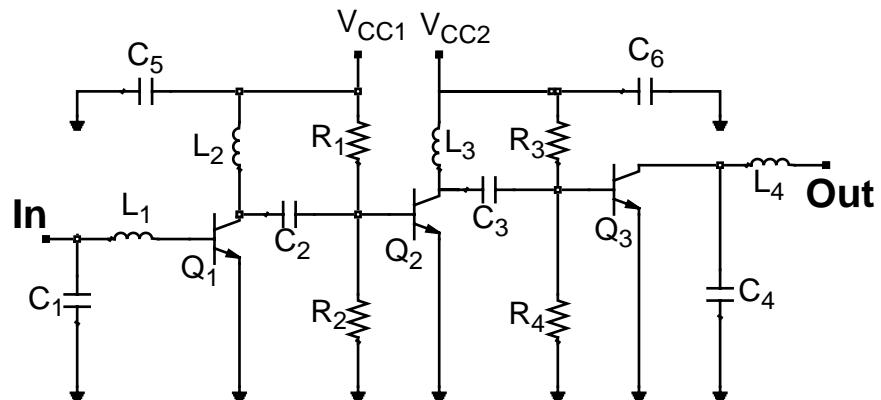
- VSWR_{in} and VSWR_{out}



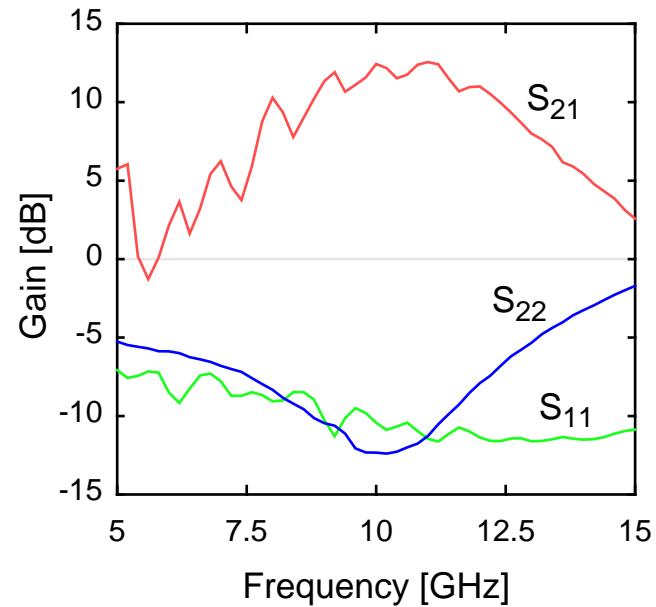
► $\text{VSWR}_{\text{in}}=1.69$
► $\text{VSWR}_{\text{out}}=1.14$

Three-stage X-band SiGe/Si Monolithic Amplifier

- Circuit Schematic



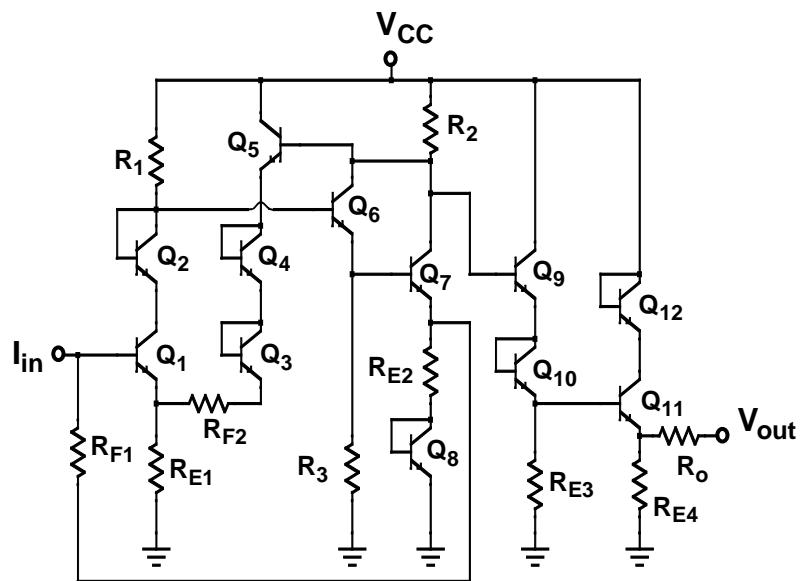
- Gain and Return Losses



- $S_{21}=12.62 \text{ dB} @ 10.0 \text{ GHz}$
- $\text{VSWR}_{\text{in}}=1.71$
- $\text{VSWR}_{\text{out}}=1.63$

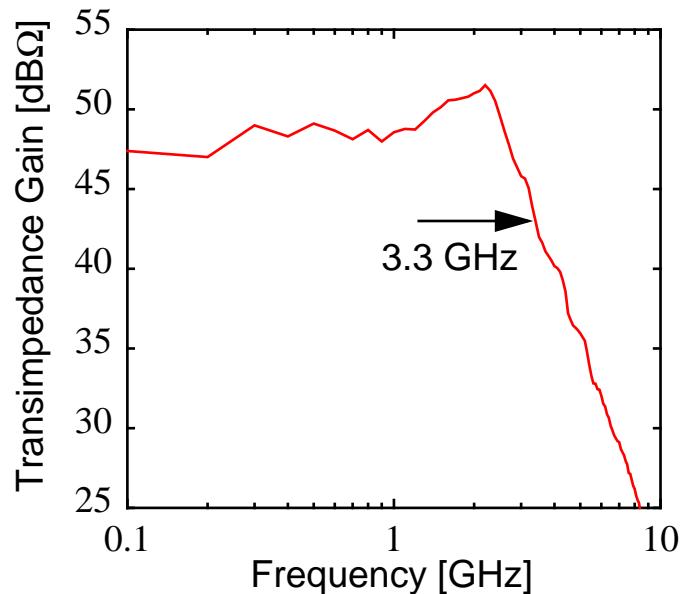
Characteristics of Dual-feedback SiGe/Si Transimpedance Amplifier

- Circuit Schematic



- $R_{F1}=200 \Omega$, $R_{F2}=150 \Omega$
 $R_{E1}= 10 \Omega$, $R_{E2}=10 \Omega$,
 $R_{E3}=700 \Omega$, $R_{E4}=550 \Omega$, $R_o=50 \Omega$
 $R_1=300 \Omega$, $R_2=100 \Omega$, $R_3=550 \Omega$

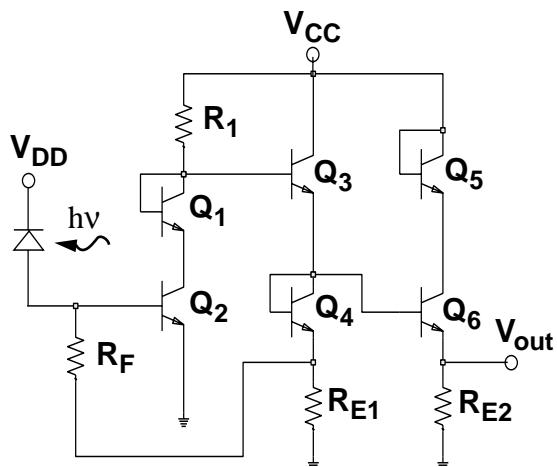
- Frequency Response



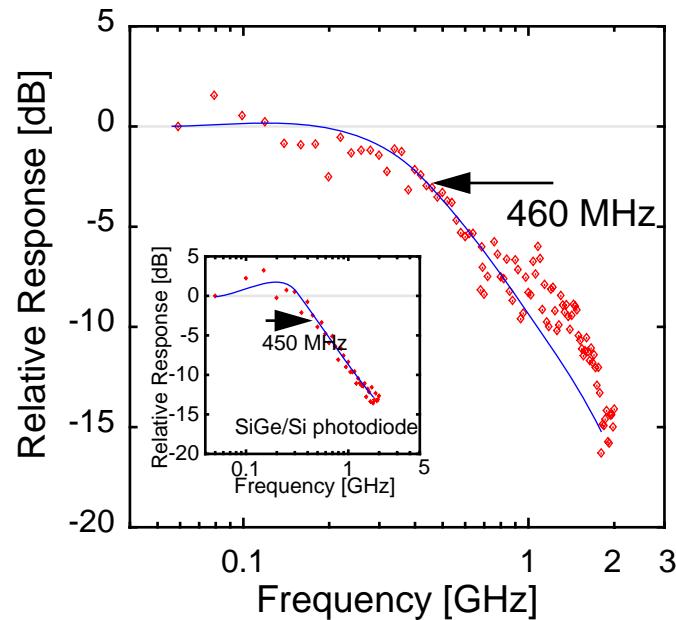
- Gain= 47.4 dBΩ
➤ BW = 3.3 GHz @ $V_{CC}= 7$ V

Characteristics of SiGe/Si PIN-HBT Photoreceiver

- Circuit Schematic



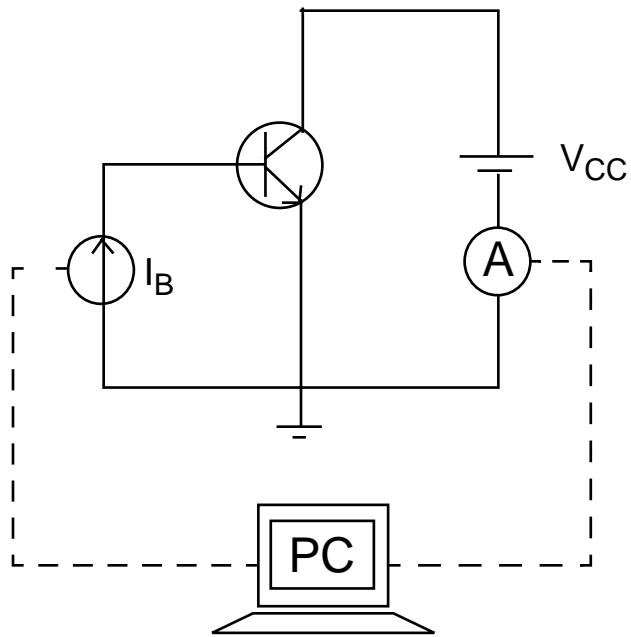
- Frequency Response



► BW = 460 MHz
@ $V_{CC}=6$ V, $V_{DD}=9$ V

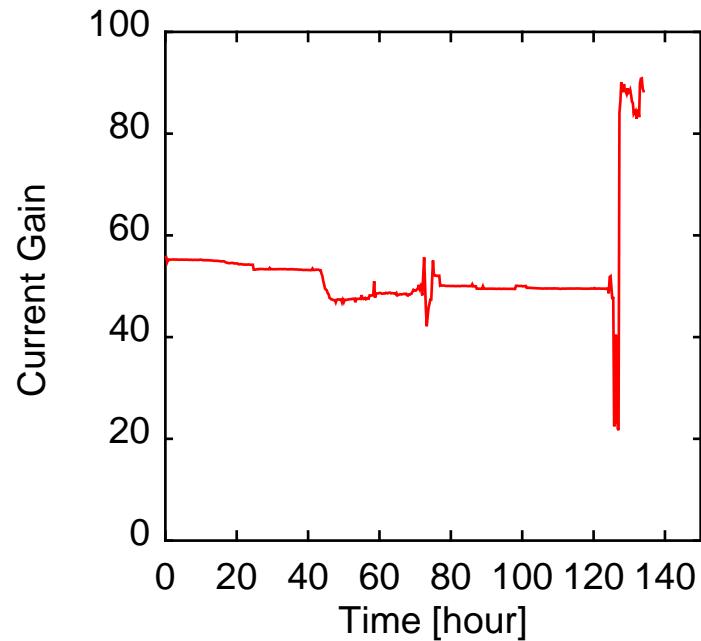
Reliability Test of SiGe/Si HBT

- Test Setup



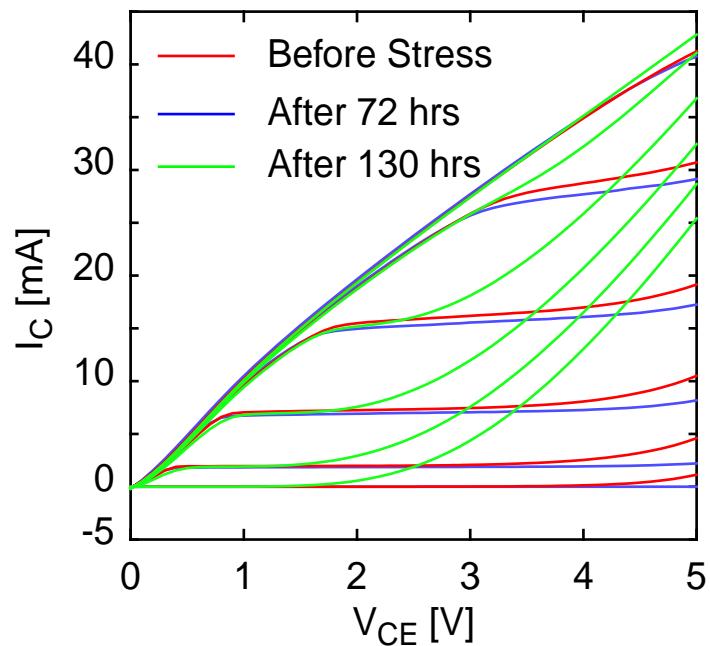
- Feedback control for constant I_C by adjusting I_B
- $V_{CC} = 3V$, $J_C = 13.5 \text{ kA/cm}^2$, $T = 175^\circ\text{C}$

- Current Gain

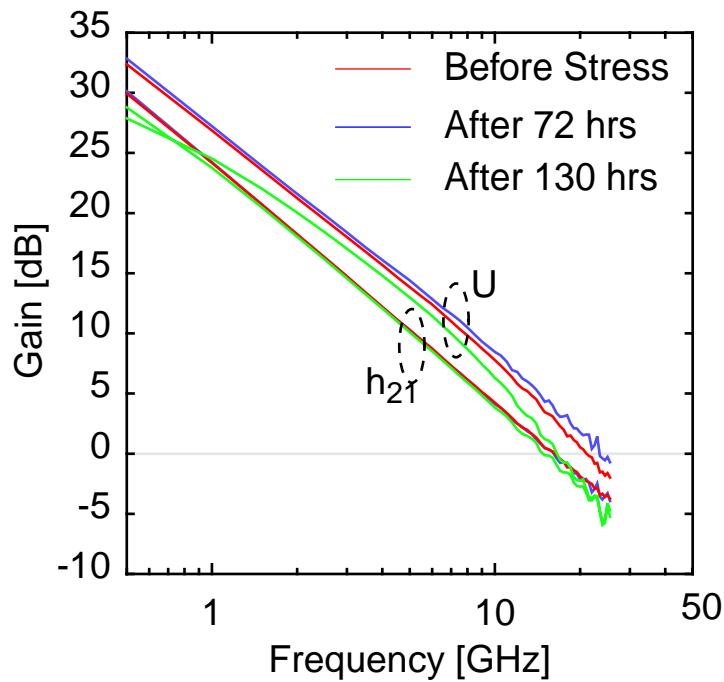


Influence of Thermal Bias Stress on HBT Characteristics

- I-V Characteristics



- Frequency Response



Specifications of SiGe/Si Power Amplifiers

- Operation Frequency

- X-band (10 GHz)
- Ka-band (30 GHz)

- Gain

- $G = 37 \text{ dB}$

- Output Power

- $P_o = 10 \text{ W}$

- Supply Voltage

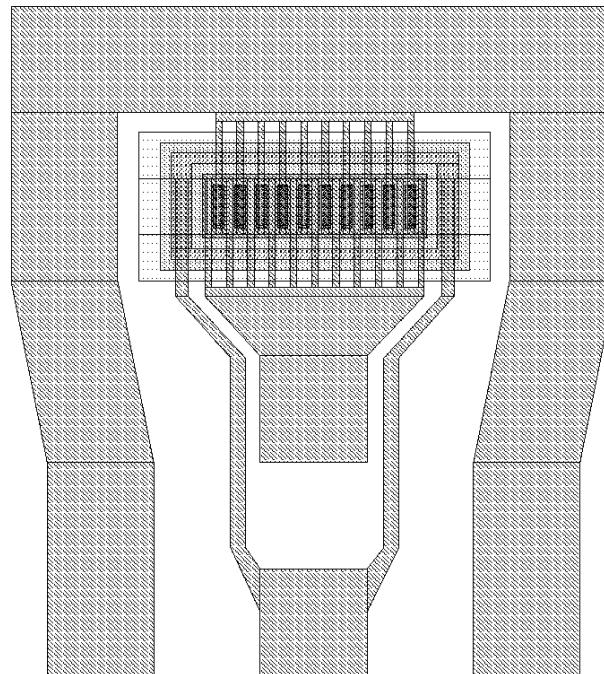
- $V_{CC} = 5 \text{ V}$

Structure of SiGe/Si Power HBT

- Epitaxial Structure

Emitter Contact	Si	n+	1e19	2000 Å
Emitter	Si	n	2e18	1000 Å
Spacer	SiGe	i		50 Å
Base	$Si_{1-x}Ge_x$	p+	1e20	200 Å
Spacer	SiGe	i		50 Å
Collector	Si	n-	1e16	4000 Å
Subcollector	Si	n+	1e19	1.5 μm
Substrate	Si	p-	2e12	540 μm

- Layout



Power HBT Design Considerations

- **Collector Doping Concentration N_C**

$$P_{max} \sim \frac{1}{8} I_{max} BV_{CEO} \text{ for Class-A operation}$$

$$I_{max} \sim qv_s A_{BC} N_C \text{ for Kirk Effect Limit } (N_C \sim N_{carrier})$$

$$BV_{CEO} \sim \frac{\epsilon_s E_C^2}{2qN_C}$$

$$\Rightarrow P_{max} \sim \frac{1}{16} v_s A_{BC} \epsilon_s E_C^2$$

$\Leftrightarrow P_{max}$ is independent or a weak function of N_C

$\Leftrightarrow N_C$ can be optimized for high speed operation

- **Collector Thickness W_C**

$$W_C \sim x_{d,max}$$

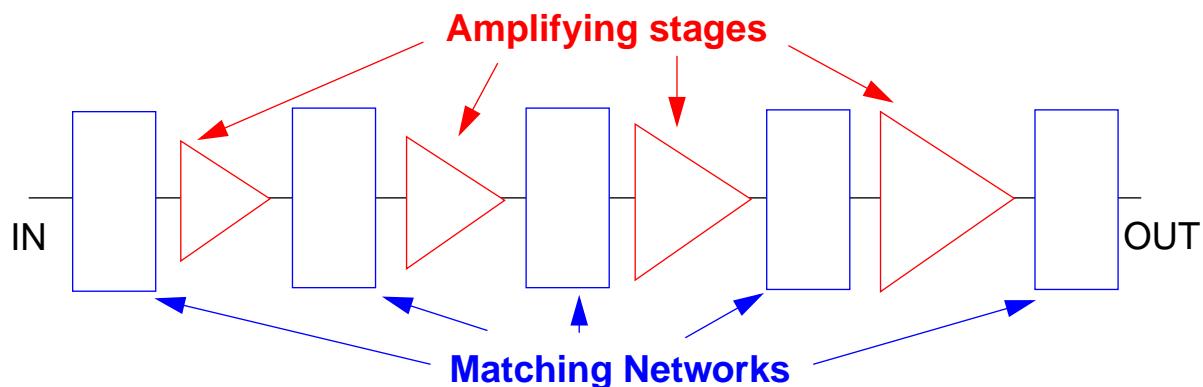
$$\sim \frac{\epsilon_s E_C}{qN_C}$$

- **BC Junction Area A_{BC}**

$$A_{BC} \sim \frac{16P_{max}}{v_s \epsilon_s E_C^2}$$

Configuration of Power Amplifier

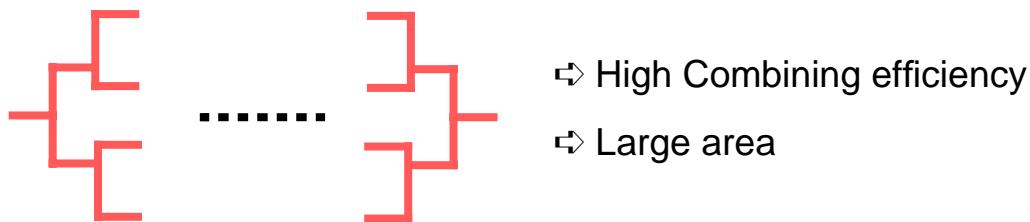
- Schematic of Power Amplifier



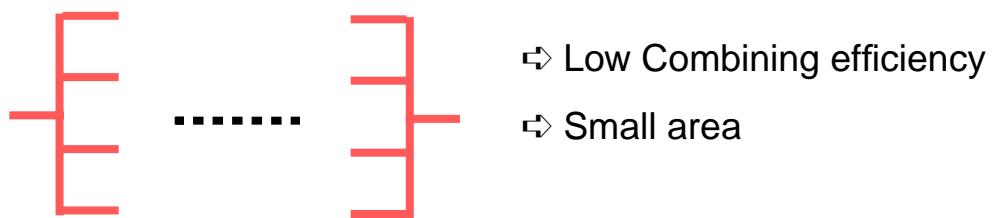
- Last stages need parallel combination of power devices
- Each stage provides 10 dB

- Parallel combination of power devices

- Binary Power Combiner/Divider



- Chain Power Combiner/Divider



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